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TO: SAFIRE / FIBRE / CSO PEOPLE

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SUBJECT: BITS, BITS, BITS… HOUSEKEEPING REDEFINITION

DATE: 2001-05-12

STATUS BITS AT THE CSO

This document will serve to modify the previous "Bits, Bits, Bits…" memo (http://pioneer.gsfc.nasa.gov/safire/internal/mail/mhonarc/safire-prototypes/msg00006.html). The definition of the housekeeping bits was reanalyzed with the intent to remove any loss-of-timing problems associated with unexpected telescope motions (e.g., from severe wind shake); see memo by Rick Shafer (http://pioneer.gsfc.nasa.gov/safire/internal/mail/mhonarc/safire-prototypes/msg00024.html). I shall summarize only the changes to the Telescope and Housekeeping status bits which will be used at the CSO for FIBRE, and, presumably, for SAFIRE.

Antenna status bits: two TTL bits for the primary mirror, "Not Idle" and "Acquired".

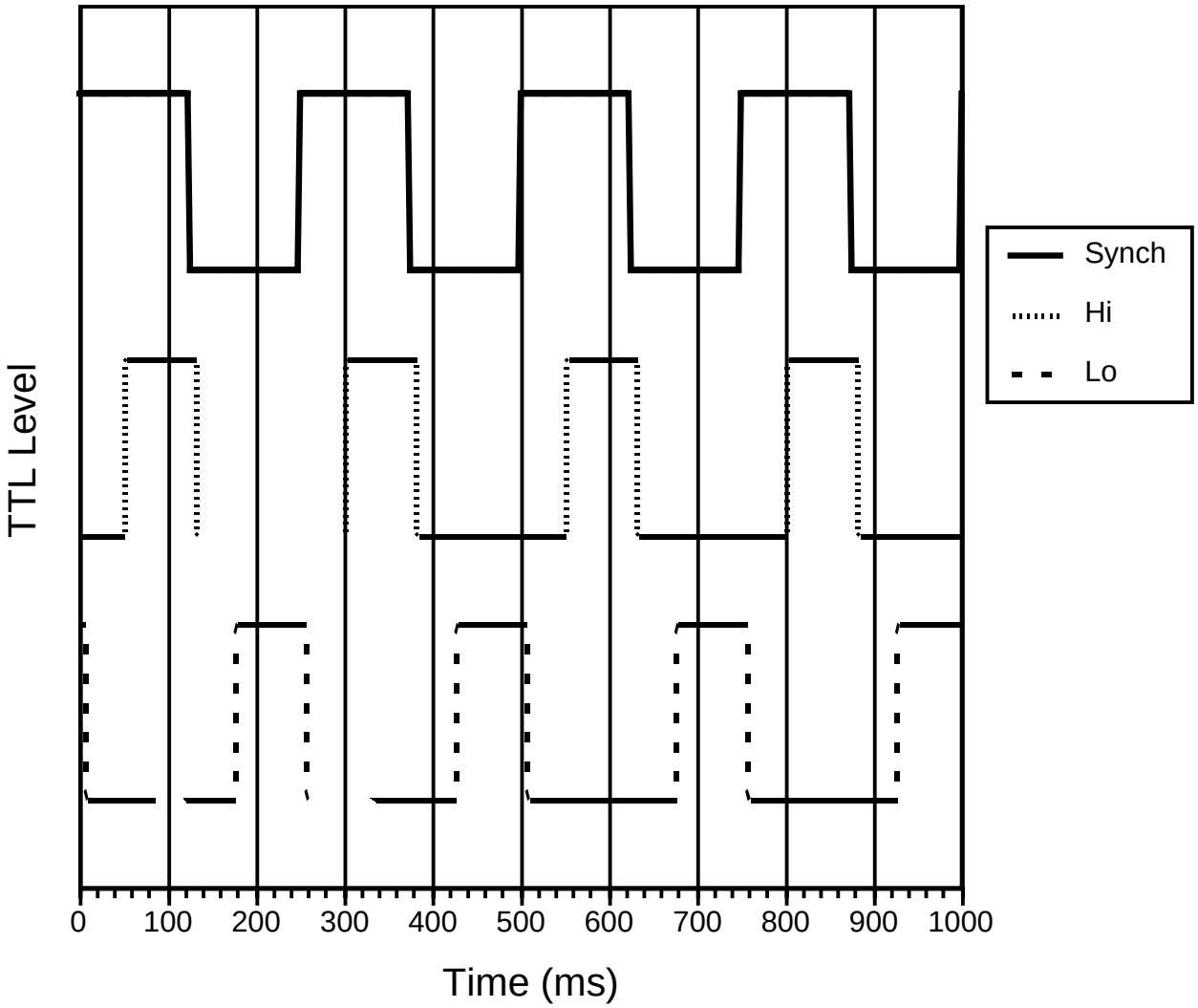
NOT IDLE	ACQ	Meaning
0	0	Telescope is not doing anything – usually not a good thing.
0	1	Telescope is pointing at a fixed position; used for drift scans.
1	0	Telescope is slewing towards a source position *or* has temporarily lost tracking.
1	1	Telescope is tracking an object on the sky.

In practice, the only time we are likely to observe is when the status is (1,1). Note that this is different from the previous memo, where I had mistakenly inverted the sense of "Idle". We must acquire the data in real time on the PC (assumed to be running the IRC and acquiring all detector data) in order that we know which data to flag as "bad" because we weren't looking anywhere useful.

Secondary status bits: three TTL bits for the secondary mirror, called "Hi", "Lo", and "Synch". The explanation should be obvious; note that I have renamed these bits from the older standard of "On" and "Off" to fit with current CSO nomenclature. Contrary to the catholic definition of "Synch", this bit is actually a square wave with 50% duty cycle that tracks the "Hi" bit fairly well. The plan as it stands now is that we will synchronize the Fabry-Perot to move on the falling edge of the "Lo" bit. This indicates the end of a single motion of the secondary mirror.

For working numbers, the following is generally true: the secondary is best used at its highest efficient frequency of 4Hz. The efficiency if roughly 35% "Hi", 35% "Lo", and 15% slewing between each position. This assumes a throw (angular separation of the beams) of approximately 60''. The maximum throw is about 240''. Being slew-rate-limited, smaller throws will yield higher efficiencies. The throw is usually chosen to be symmetric about the pointing axis of the primary mirror, but the fraction of time spent in each beam is not precisely identical.

Here's a schematic timing diagram for the secondary status bits, based on actual measurements:

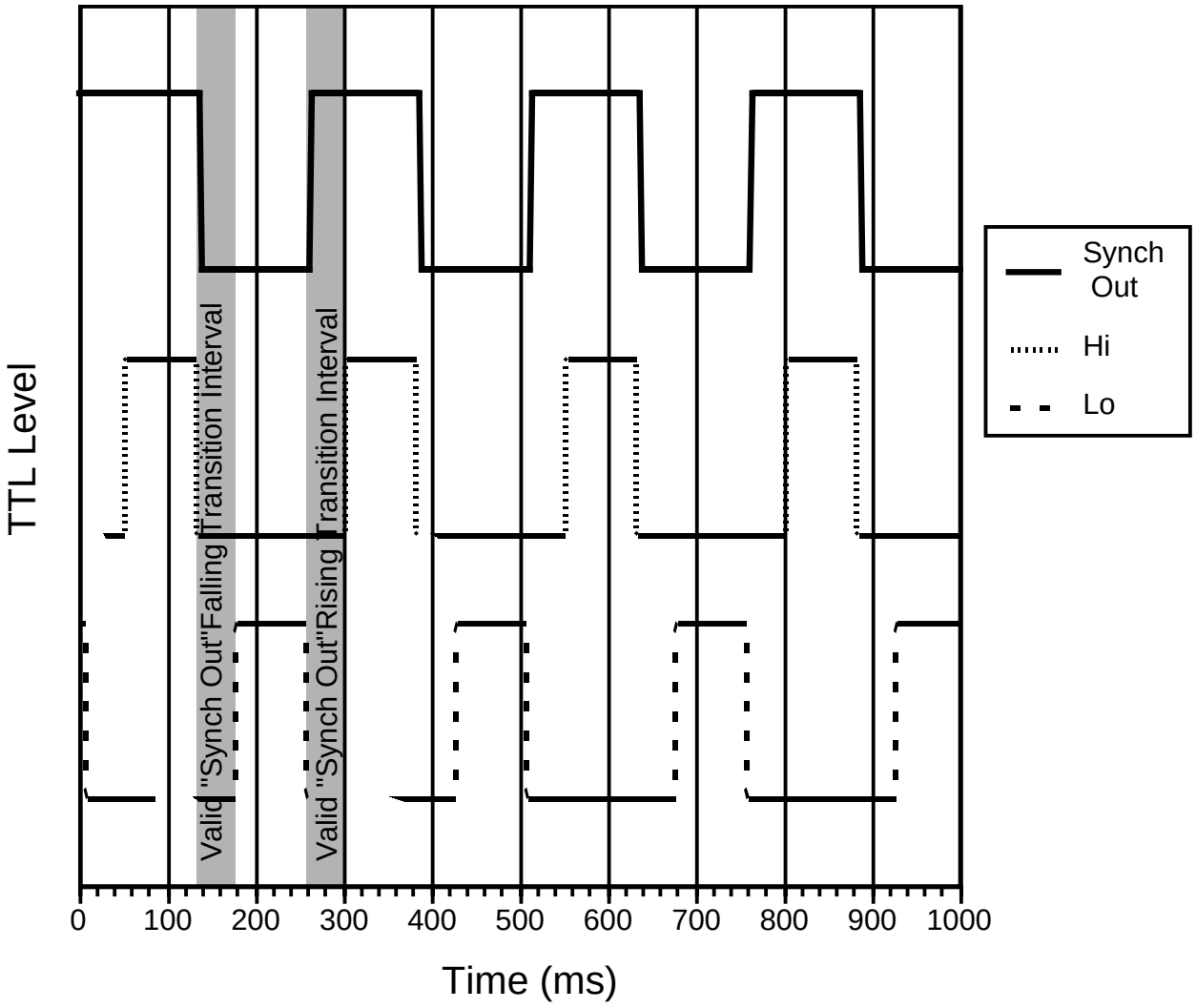


The readily apparent problem is that the Synch bit is out of phase with the actual motion of the secondary mirror. This phase delay is variable and will depend on throw, frequency, and secondary control loop tuning. Furthermore, poor tuning can result in glitches where the Hi and Lo bits will flip low in the middle of their normally-high period.

What we need is a bit that represents the motion of the secondary in the following way: the bit must go high on the rising edge of "Hi" and must go low on the rising edge of "Lo". In fact,

this is exactly the function of the "Synch" bit with the phase delay removed. The problem is that there is no easy way of automatically removing this phase delay: it depends on parameters chosen by humans. Furthermore, it is not robust to generate a properly synchronized bit from the "Hi" and "Lo" bits, since they can glitch too easily. It might be possible to generate the appropriate bit with a phase-locked loop, but this is always a little iffy. I propose that we incorporate a tunable delay generator into the "Synch" bit which can be adjusted by standard monkey-in-the-loop practices. Lest anyone feel this is a bit of a comedown, bear in mind that tuning the secondary mirror is a 4-parameter problem; this will bring it to 5-params. SHARC requires 6 knobs to be tweaked to provide proper secondary motion!

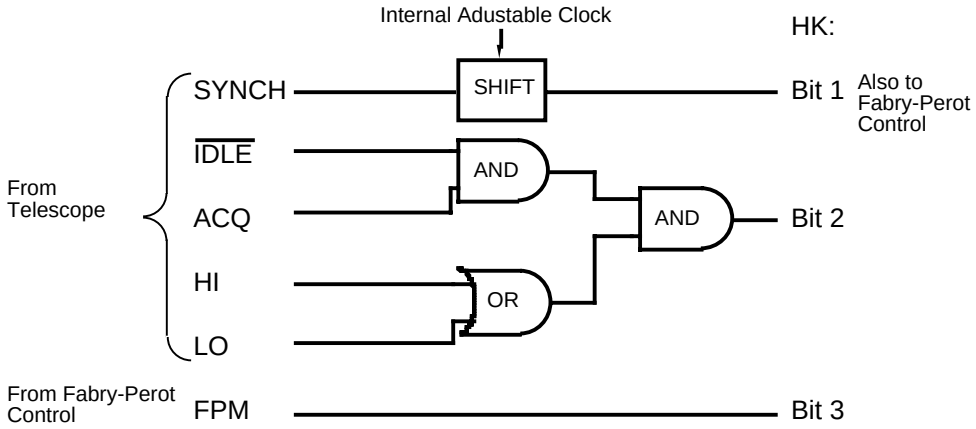
My proposed method of implementing a delay is to introduce an asynchronously-clocked shift register into the "Synch" line, and to allow the operator to change the clock rate. For all forseeable phase errors, I believe a clock operating at 100Hz-1kHz with an 8-bit register will suffice to provide a stable, tunable delay. This may result in jitter (1ms-10ms), but not of timescales which would result in errors in the data stream. The resulting "Synch Out" bit must be adjusted such that both its transitions fall in the region where both "Hi" and "Lo" are low, and as close as possible to the falling edge of "Lo", as shown below:



As you can see, there is plenty of slop in the timing of the "Synch Out" delay. In the above example, the interval is approximately 40ms (although 50ms is more realistic). If we assume that the Fabry-Perot can step in 25ms, the actual timing slop and jitter should be less than 25ms. The circuit diagram for the delay, along with the rest of the FIBRE Bit Box, is attached to this document.

Fabry-Perot bits: The Fabry-Perot must communicate to the PC when it moves. In addition to sending out the 16 bits to the control card, the Mac controlling the Fabry-Perot (FP) will have to send a single bit which I shall call "FP Moving" to the PC as HK (Housekeeping) Bit 3. I propose that the bit be set high before the FP is commanded, then sent low when the FP commands have all been issued.

The data acquisition system will need to use all of the above bits to know what to do with the data stream. I propose the following scheme:



Bit 1 is the "Synch" which has the following property (thanks to Rick for this formalism):

> It is high whenever "Hi" is high; it is low whenever "Lo" is high; it is synchronized with the secondary mirror motion so that its rising transition can trigger the Fabry-Perot to move.

Bit 2 is the "Valid Data" bit, and has the properties:

> It is high when the telescope and secondary mirror are pointing at something we're interested in; it is low when any of the moving parts of the telescope is not pointing at something interesting.

When the IRC processes and stores data, the plan is to perform a realtime coaddition of data in "On" and "Off" registers for each detector. The HK Bits 1 and 2 determine how this is done. If Bit 2 is low, the data is junk; if it is high, the data must be stored. When Bit 1 is high, accumulate data in the "On" register when in the 1st and 4th part of the Nod cycle, in the "Off" register when in the 2nd and 3rd parts of the Nod cycle. When Bit 1 is low, accumulate data in the "Off" register when in the 1st and 4th part of the Nod cycle, in the "On" register when in the 2nd and 3rd parts of the Nod cycle.

The truth table for bits 1 and 2 is as follows:

NOT IDLE	ACQ	HI	LO	Bit 1	Bit 2
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0*	1*
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	0*	1*
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	0*	1*
1	1	0	0	0	0
1	**1**	**0**	**1**	**1**	**0**
1	**1**	**1**	**0**	**1**	**1**
1	1	1	1	1*	1*

* The electronics which generate the "Hi" and "Lo" bits should *never* yield (1,1). Actually, I suspect that technically, they could generate (1,1) if the operator requests that the chopper throw be 0''. Whatever happens in this event is the fault of that operator.

Notes:
- One side panel has 6 isolated BNC inputs
- Opposite side panel has 3 isolated BNC outputs with adjacent status LEDs
- One end panel has BNC "Synch Check" output, one 10-turn pot for clock adjustment, and sonic alert reset pushbutton
- One end panel has BNC power input and locking SPST power switch
- All digital chips should be TTl types (74LS, 74ALS, 74F) and must be mounted into sockets with integral capacitors.
- Sonic alert placed inside box.

TITLE: FIBRE Telescope Interface

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